Topologically Homogeneous Power-Performance Heterogeneous Multicore (THPH) Systems

Koushik Chakraborty
Sanghamitra Roy

Electrical and Computer Engineering
Utah State University
Outline

• Background
  – Power Consumption in CMOS devices

• Motivation

• THPH Multicore
  – Selecting VF Domains
  – Runtime Adaptation

• Results

Work received a Best Paper Award nomination at Design Automation and Test in Europe (DATE) 2011
Background

• Dynamic Power
  \[ P_D = C \times V_{DD}^2 \times F \times \alpha \]

• Static Power
  \[ P_S \propto \exp(-Vth) \]

• Technology Scaling Impact
Dynamic Voltage and Frequency Scaling (DVFS)

• Key technology for energy efficiency
• Basic Idea: adapt certain circuit parameters during low utilization
  – Reduce performance levels (*frequency*)
  – Commensurate reduction in supply voltage
  – Offers cubic reduction in dynamic power
• All commodity multicores have DVFS capability
Motivation

• Energy Efficiency: a key to modern systems
• Modular designs leading to growing replicated components
• Diversity in application characteristics
  – Demanding distinct power-performance tradeoffs from the hardware

Dynamic Voltage Frequency Scaling (DVFS) extensively used to mitigate energy efficiency degradation
DVFS Inefficiency: Technology Trend

• DVFS becoming inefficient with scaling
  – Voltage scaling margin shrinking
    • Due to reliability and leakage concerns
  – Dynamic adaptation unable to alter the underlying circuit characteristics
    • gate size and threshold voltage tuned for nominal frequency: inherently power hungry
DVFS Inefficiency

- 32 bit ALU from ISCAS benchmark suite
- 20% Voltage scaling
- Normalized energy efficiency of DVFS wrt latency optimal designs

Latency optimal designs more energy efficient than DVFS scaled counterparts by up to 5.9X
THPH Paradigm: Circuit Designs tuned for target latency

• Replicated components designed for different target latencies

• Enables appropriate choice of physical design parameters
  – Gate size (Capacitance)
  – Threshold voltage (Leakage during active cycles)
How to adapt multicore system design

• Objectives:
  – Maintain identical architectural symmetry
    • No change in RTL
  – Design individual components for separate target performance
Traditional design: all cores tuned for nominal VF 1V, 3Ghz

THPH design: Cores tuned for separate VF levels

<table>
<thead>
<tr>
<th>Cluster</th>
<th>Core configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Core 0: 1V, 3Ghz</td>
</tr>
<tr>
<td></td>
<td>Core 1: 0.84V, 2.4Ghz</td>
</tr>
<tr>
<td>1</td>
<td>Core 0: 1V, 3Ghz</td>
</tr>
<tr>
<td></td>
<td>Core 1: 0.81V, 2Ghz</td>
</tr>
<tr>
<td>2</td>
<td>Core 0: 0.84V, 2.4Ghz</td>
</tr>
<tr>
<td></td>
<td>Core 1: 0.81V, 2Ghz</td>
</tr>
<tr>
<td>3</td>
<td>Core 0: 0.81V, 1.8Ghz</td>
</tr>
<tr>
<td></td>
<td>Core 1 0.81V, 1.5Ghz</td>
</tr>
</tbody>
</table>
Key Design Issues

• Selecting VF Domains
• Runtime Adaptation
VF Domain Algorithm

• Given a set of $k$ VF domain levels
• Select VF domain assignment for $n$ cores
  – Maximize system level energy efficiency
• Workload space
  – $p$ IPC classes $\rightarrow$ Workload space $p^n$
  – Exponential complexity

Use Simulated Annealing based Stochastic Optimization
Simulated Annealing Formulation

\[
\begin{align*}
\text{minimize} & \quad \sum_{i=1}^{n} E(F_i(\nu)) \\
\text{s.t.} & \quad Y(\nu) \geq Y_0
\end{align*}
\]

• Where \( \sum_{i=1}^{n} E(F_i(\nu)) \) is a regression model of Energy as a function of the core frequency \( F_i \)

• \( Y(\nu) \) is Multicore Performance Yield to estimate the performance loss in a large workload space
Multicore Performance Yield

\[ Y(\nu) = \Pr\left( \frac{1}{n} \sum_{i=1}^{n} \frac{IPC_i(\nu)}{IPC_{\text{base}}} \geq L_0 \right) \]

- Probability that a VF assignment \( \nu \) produces a relative performance higher than \( L_0 \) under diverse workload conditions
- Estimated using Monte Carlo simulations
SA Formulation

- Traditional annealing schedule
  - Temperature initialized to high value $T_0$ and cools down to $\varepsilon$
  - Initial solution: All cores with highest VF setting
  - Moves: Randomly select a VF domain and
    - Raise to next higher level
    - Lower to immediate lower level
Implementation

• Runtime Adaptation
  – Hardware task migration – Reassign workloads on available THPH cores to better fit their runtime characteristics

• Overhead
  – Saving and restoring register state
  – Loss of branch predictor state
  – Cold cache (only for inter-cluster migration)
Methodology

• Full system simulation based on SIMICS
• Benchmarks – Consolidated Virtual Machines composed of SPEC CPU2006 applications
• 64 bit out-of-order microprocessor core
  – Verilog modeling and synthesis
• Power-Performance Simulation
  – Power from ASIC standard cell flow combined with usage from architectural simulator
• Temperature - Power data fed to Hotspot
Comparative Schemes

• Homogeneous cores with DVFS – **D-DVFS**
• Homogeneous cores with static VF - **SVFS**
• **THPH**
• THPH with task migration - **THPH-TM**
## Comparative Schemes

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Task Migration</th>
<th>Overhead</th>
<th>Power Efficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-DVFS</td>
<td>No</td>
<td>VF transition delay</td>
<td>No</td>
</tr>
<tr>
<td>SVFS</td>
<td>Yes</td>
<td>Task migration</td>
<td>No</td>
</tr>
<tr>
<td>THPH</td>
<td>No</td>
<td>VF transition delay</td>
<td>Yes</td>
</tr>
<tr>
<td>THPH-TM</td>
<td>Yes</td>
<td>Task migration</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Results - Throughput

Higher is better
Results – Energy Efficiency

Higher is better
Conclusion

• THPH Multicore Design Paradigm
  – Captures application diversity
  – Tackles growing inefficiency of DVFS

• Observed benefits in energy efficiency and thermal characteristics
Thank You!